

Condura®.ultra

Ag free Active Metal Brazed (AMB) Si₃N₄ Substrates Design Guidelines



AMB-Si₃N₄ Product Facts

- Silicon nitride ceramic
Thicknesses: 0.25 mm / 0.32 mm
- Active Metal Brazed OFE Cu (oxygen-free)
Thicknesses: 0.30 mm / 0.40mm / 0.50 mm / 0.80 mm
(Other thicknesses on request)
- Asymmetric brazing is possible: copper front side to back side with a max. difference of 0.10 mm is possible
- Delivery as single unit or mastercard is possible
- Surface finish: Bare Cu, full or selective Ag plating

Key features

- Ag free AMB technology
- Cost effective high performance substrate
- Thermal conductivity of ≥ 80 W/m.K
- Enables thick Cu layers (e.g. 0.8 mm)
- Special treatments possible to adjust surface properties

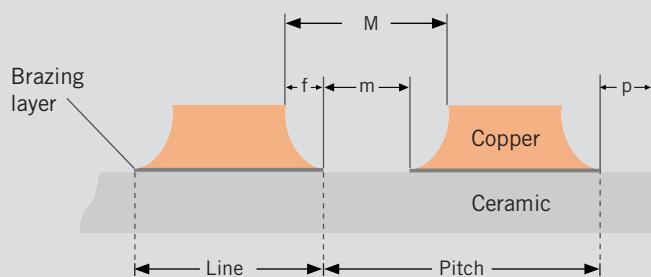
Si₃N₄ Material Properties

	Rating	Unit
Bending strength	≥ 650	MPa
Fracture toughness	≥ 6	MPa·m ^{1/2}
Thermal conductivity (@ 20 °C)	≥ 80	W/m·K
Coefficient of thermal expansion (20 °C - 500 °C)	typ. 2.6 ppm	1/K
Young's modulus (@ 20 °C)	≥ 280	GPa
Electrical strength (@ 50Hz)	≥ 20	kV/mm
Dielectric resistivity (@ 20 °C)	$\geq 10^{14}$	Ω ·cm

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Etching Properties



m = metal-free distance (Space)
 f = flank
 M = iso-groove opening Cu top
 p = metal-free perimeter

Structuring

Thickness Cu [mm]	Min. metal-free distance (m) [mm]	Min. line [mm]	Min. pitch [mm]
0.30	0.50	0.50	1.00
0.40	0.60	0.60	1.20
0.50	0.70	0.70	1.40
0.80	1.00	1.00	2.00

Structuring tolerance

Thickness Cu [mm]	Tolerance of structuring dimensions referring to (m) [mm]
0.30	± 0.20
0.40	± 0.25
0.50	± 0.30
0.80	± 0.40

All isolation gaps in a layout should have the same dimension. Isolation gaps with different dimensions may result in larger etching tolerances.

Metal-free perimeter

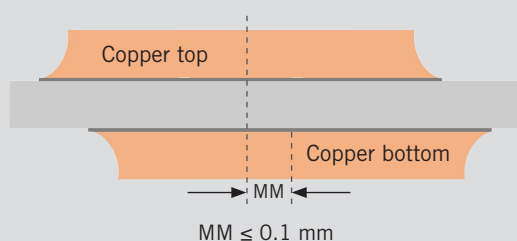
Thickness Cu [mm]	Min. Metal-free perimeter (p) [mm]
0.30	0.25
0.40	0.30
0.50	0.35
0.80	0.50

Sidewall of structured pattern (flank)

Thickness Cu [mm]	Flank (f)
0.30 - 0.80	$\leq \frac{1}{2}$ Thickness Cu

Tolerance of metal-free perimeter depends on ceramic thickness and manufacturing tolerances.

Mismatch Top to Bottom Copper



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Substrate Characteristics

Mastercard / Single unit dimension & tolerances

Mastercard usable area	178mm · 127 mm
Single unit dimension*	≥ 15 mm · 15 mm
Tolerances	+0.2 / -0.05 mm

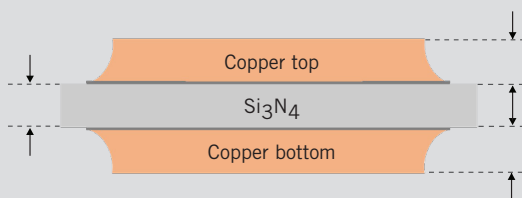
*Smaller dimensions on request

Warpage behavior depends on specific layout, single unit size and material combination and can only be specified after initial sample preparation.

Thickness tolerances

Total thickness (Cu+Si₃N₄+Cu) tolerance	± 10 %
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Thickness combinations



Si ₃ N ₄ Thickness (mm)	Cu Thickness* (mm)			
	0.3	0.4	0.5	0.8
0.32	√	√	√	√
0.25	√	√	√	N/A

* Other combinations incl. asymmetric on request.

Surface plating

Plating	Thickness (um)
Ag (immersion silver)	0.30 - 1.00

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Metal and hole properties

Surface roughness*

$R_a < 1.5 \mu\text{m}$, $R_z < 10 \mu\text{m}$

*Different roughness on request

Copper peeling strength

$> 6.8 \text{ N/mm}$

Note: Internal test with 0.30 mm Cu

Customized surfaces

Heraeus Electronics offers collaborative development initiatives with focus on the optimization of surfaces and process parameters for various assembly techniques including:

- Silver sintering
- Solder wetting
- Heavy wire bondability
- Increased die shear strength

Technology and Application Centers

Besides offering Assembly Materials, Bonding Wires and Metal Ceramic Substrates, Heraeus Electronics provides matching material solutions and R&D oriented partnerships to create individual solutions.

Heraeus Electronics offers the following Metal Ceramic Substrates and Services:

- IATF 16949 certified supply of:
 - ✓ Condura[®].ultra AMB-Si₃N₄ (Ag-free Active Metal Brazed Si₃N₄)
 - ✓ Condura[®].prime AMB-Si₃N₄ (Active Metal Brazed Si₃N₄)
 - ✓ Condura[®].extra DCB-ZTA (Zirconia-toughened Alumina)
 - ✓ Condura[®].classic DCB-Al₂O₃ (Direct Copper Bonded Al₂O₃)
- Engineering Services:
 - ✓ Simulation, Prototype Design & Assembly, Testing and Qualification, Material Analysis

Heraeus Electronics does not take responsibility for the final layout design. This document offers only Design Guidelines for the substrate layout.

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