

## Condura®.classic

### Alumina Direct Copper Bonding (DCB) Substrates Design Guidelines



#### Alumina DCB facts

- Alumina ceramic Al<sub>2</sub>O<sub>3</sub> (96 %) Thicknesses<sup>(1)</sup>: 0.38 mm / 0.63 mm
- Direct Copper Bonding Cu-OFE Thicknesses<sup>(1)</sup>: 0.2 mm / 0.25 mm / 0.3 mm / 0.4 mm
- Single unit or master card size 7" x 5" (usable area)
- Surface finish: Bare Cu, Ni, Ni / Au, full or selective Ag plating

(1) Different material combinations on request

#### Key features

- Good thermal and mechanical properties
- Low coefficient of thermal expansion (CTE)
- Special treatments possible to adjust surface properties

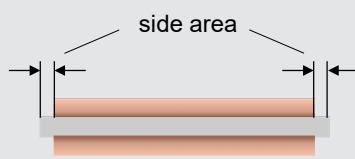
#### Al<sub>2</sub>O<sub>3</sub> material properties

	Rating	Unit
Bending strength	≥ 450	N/mm <sup>2</sup>
Thermal conductivity (@ 20 °C)	≥ 20	W/m-K
Coefficient of thermal expansion (100 °C - 600 °C)	6.7 - 8.7 ppm	1/K
Young's modulus (@ 20 °C)	≥ 300	GPa
Density	≥ 3.73	g/cm <sup>3</sup>
Electrical resistivity	≥ 10 <sup>13</sup>	Ohm.cm
Dielectric strength	≥ 15	kV/mm

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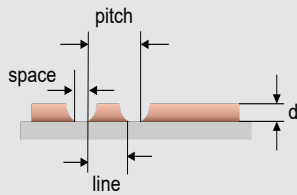
### Copper free area



Thickness Cu [mm]	Min. side area [mm]
0.20	0.20
0.25	0.23
0.30	0.25
0.40	0.35

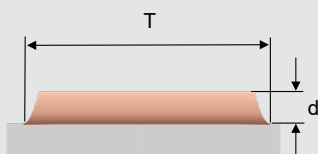
Tolerance of copper-free perimeter depends on ceramic thickness and manufacturing tolerances.

### Structuring



Thickness Cu [mm]	Min. space [mm]	Min. line [mm]	Min. pitch [mm]
0.20	0.40	0.40	0.80
0.25	0.45	0.45	0.90
0.30	0.50	0.50	1.00
0.40	0.60	0.60	1.20

### Etching tolerance



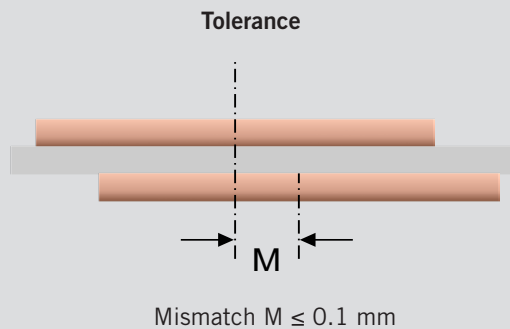
Tolerance length & width [mm]	Thickness Cu [mm]
T <sub>typ.</sub> = ± 0.15	d = 0.2
T <sub>typ.</sub> = ± 0.20	d ≤ 0.3
T <sub>typ.</sub> = ± 0.20	d ≤ 0.4

All isolation gaps in a layout should have the same dimension. Isolation gaps with different dimensions may result in larger etching tolerances.

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### Tolerance



Tolerance of total thickness = + 7 % / -10 %

### Dimensions

General dimensions	Rating [mm]	Tolerances of single parts	Rating [mm]
Max. usable area	127 x 178	Ceramic thickness $\leq 0.63 \text{ mm}$	+ 200 $\mu\text{m}$ - 50 $\mu\text{m}$
Minimum dimension for ceramic thickness $\leq 0.63 \text{ mm}$	10 x 10 (smaller on request)		

Warpage behavior depends on specific layout, single part size and material combination and can only be specified after initial sample preparation.

### Thickness combinations

Al <sub>2</sub> O <sub>3</sub> Thickness [mm]	Cu Thickness* [mm]			
	0.20	0.25	0.30	0.40
0.63	√	√	√	√
0.38	√	√	√	N/A

\* Other combinations incl. asymmetric on request.

### Surface plating

Plating Method	Thickness ( $\mu\text{m}$ )
Electroless Ni	3 - 7 (9% $\pm$ 2 % P)
Electroless NiAu	Ni 3 - 7 (9% $\pm$ 2 % P) Au Class 1: 0.01 - 0.05 Au Class 2: 0.03 - 0.13

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### Metal and hole properties

Surface roughness*	Minimum hole diameter
Rmax = 50 µm	d <sub>hole</sub> = 1 mm
Ra ≤ 1 µm	Electrical conductivity raw copper
Rz ≤ 16 µm	G <sub>Cu</sub> = 58 · 10 <sup>6</sup> S/m
	Thickness Cu    Copper peeling strength
	0.30 mm            > 4 N/mm

\*Different roughness on request

### Technology and Application Centers

Besides offering Assembly Materials, Bonding Wires and Metal Ceramic Substrates, Heraeus Electronics provides matching material solutions and R&D oriented partnerships to create individual solutions.

### Customized surfaces

Heraeus Electronics offers collaborative development initiatives with focus on the optimization of surfaces and process parameters for various assembly techniques including:

- Silver sintering
- Solder wetting
- Heavy wire bondability
- Increased die shear strength

#### Heraeus Electronics offers the following Metal Ceramic Substrates and Services:

- IATF 16949 certified supply of:
  - ✓ Condura®.ultra AMB-Si<sub>3</sub>N<sub>4</sub> (Ag-free Active Metal Brazed Si<sub>3</sub>N<sub>4</sub>)
  - ✓ Condura®.prime AMB-Si<sub>3</sub>N<sub>4</sub> (Active Metal Brazed Si<sub>3</sub>N<sub>4</sub>)
  - ✓ Condura®.extra DCB-ZTA (Zirconia-toughened Alumina)
  - ✓ Condura®.classic DCB-Al<sub>2</sub>O<sub>3</sub> (Direct Copper Bonded Al<sub>2</sub>O<sub>3</sub>)
- Engineering Services:
  - ✓ Simulation, Prototype Design & Assembly, Testing and Qualification, Material Analysis

Heraeus Electronics does not take responsibility for the final layout design. This document offers only Design Guidelines for the substrate layout.

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